WHAT IS CLAIMED IS:

1. A time/space switching component with multiple functionality comprising:

a time switching unit for a time allocation of a plurality of data channels;

a space switching unit for a space allocation of said plurality of data channels;

a data channel sequence correction unit correcting a time sequence of said plurality of data channels; and

a control unit driving a unit selected from the group consisting of said time switching unit, said space switching unit and said data channel sequence correction unit dependent on a selected operating mode.

2. The time/space switching component according to claim 1, wherein said time switching unit comprises:

N memory devices for storing said plurality of data channels of a time frame in a plurality of memory cells; and

N address selection stages for a selective drive of said plurality of memory cells.

3. The time /space switching component according to claim 1, wherein said space coupling unit comprises:

a line matrix with N x (N x M) connecting lines; and

M space switching selection stages for a selection of one of said N connecting lines dependent on said control unit.

4. The time /space switching component according to claim 2, wherein said data channel sequence correction unit comprises:

N bypass lines for respectively bypassing said N memory devices;

N bypass selection stages for a selective selection of either said bypass lines or said the memory devices; and

N connection selection stages for a selective, paired connection of said N memory devices to their appertaining bypass lines and for a selective selection of said memory devices with bypass lines connected in pairs dependent on said control unit.

5. The time /space switching component according to claim 3, wherein said data channel sequence correction unit comprises:

N bypass lines for respectively bypassing said N memory devices;

N bypass selection stages for a selective selection of either said bypass lines or said the memory devices; and

N connection selection stages for a selective, paired connection of said N memory devices to their appertaining bypass lines and for a selective selection of said memory devices with bypass lines connected in pairs dependent on said control unit.

6. The time /space switching component according to claim 4, wherein said N connection selection stages comprise:

N/2 input multiplexers; and

N/2 output multiplexers.

7. The time /space switching component according to claim 5, wherein said N connection selection stages comprise:

N/2 input multiplexers; and

N/2 output multiplexers.

8. The time /space switching component according to claim 2, wherein said address selection stages are multiplexers.

9. The time /space switching component according to claim 3, wherein said space switching selection stages are multiplexers.

10. The time /space switching component according to claim 4, wherein said bypass switching selection stages are multiplexers.

11. The time /space switching component according to claim 1, wherein said control unit comprises M control stages.

12. The time /space switching component according to claim 1, wherein said control unit drives a unit selected from the group consisting of said time switching unit, said space switching unit and said data channel sequence correction units such that, in a first operating mode, a time and space allocation of said plurality of data channels of N input lines onto M output lines occurs.

13. The time /space switching component according to claim 12, wherein N connection selection stages and the N bypass selection stages are deactivated.

14. The time /space switching component according to claim 1, wherein said control unit drives a unit selected from the group consisting of said time switching unit, said space switching unit and said data channel sequence correction units such that, in a second operating mode, a correction of a data channel sequence and a space allocation of said plurality of data channels occurs from N input lines onto M output lines.

15. The time /space switching component according to claim 14, wherein N connection selection stages are deactivated and N bypass selection stages are activated.

16. The time /space switching component according to claim 1, wherein said control unit drives a unit selected from the group consisting of said time switching unit, said space switching unit and said data channel sequence correction units such that, in a third operating mode, a correction of the data channel sequence as well as a time and space allocation of said plurality of data channels occurs from N/2 input lines onto M output lines.

17. The time /space switching component according to claim 16, wherein N connection selection stages are activated and N bypass selection stages are deactivated.